

Pro-One

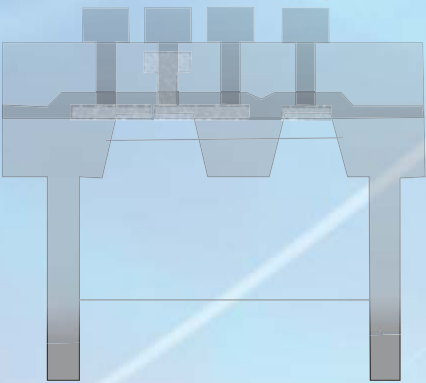


GATE

Graduate Aptitude Test in Engineering

Electronics and Communication Engineering

Digital Circuits



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DIGITAL CIRCUITS THEORY

Logic families:

There are two types of logic family

- (a) Bipolar logic family
- (b) MOS logic family

| Bipolar logic family | MOS logic family |
|--------------------------------------|-------------------|
| (i) Transistor-transistor logic(TTL) | (i) PMOS family |
| (ii) Diode-transistor logic(DTL) | (ii) NMOS family |
| (iii) Emitter coupled logic(ECL) | (iii) CMOS family |
| (iv) Current mode logic(CML) | |
| (v) Integrated injection logic(III) | |

| Logic family | Advantages |
|--------------|----------------------------------------------|
| (i) TTL | (i) In general it is high speed family |
| (ii) CMOS | (ii) Low power consumption, low speed family |
| (iii) ECL | (iii) Fastest logic family |

- **Programmable logic devices(PLD's)**

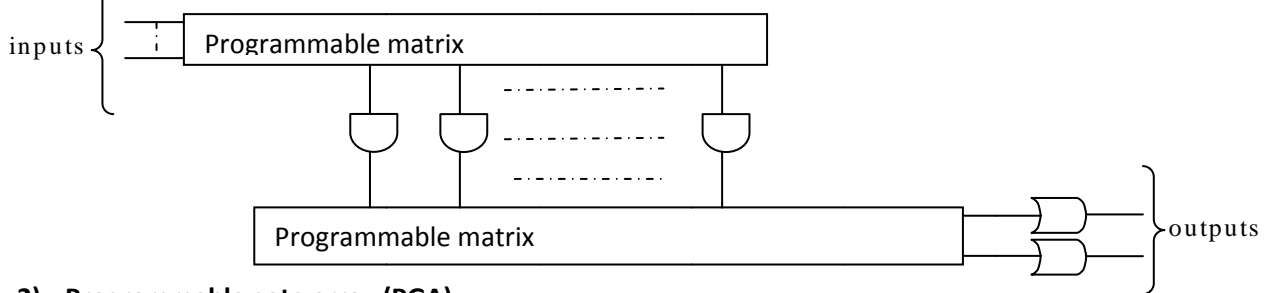
Based on technology used, there are two broad categories of PLD.

- (1) Programmable logic array(PLA)
- (2) PGA(programmable gate array)

1) Programmable logic array(PLA)

It enables logic functions expressed in SUM of products forms to be implemented directly. It consists of programmable 'AND' array at input and programmable 'OR' array at output.

Diagrammatically it can be shown as below.



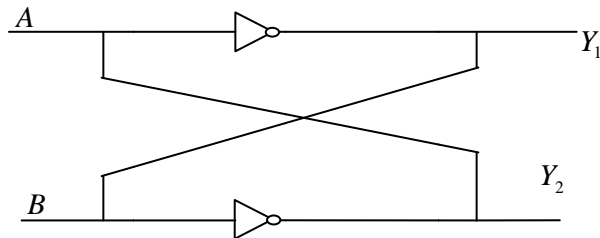
2) Programmable gate array (PGA)

PGA is semicustom devices based on array of simple cells selected from a library surrounded by an interconnection network. It subdividing array into building blocks performing higher order logic functions rather than individual gates. These cells at macro-level called macro-cell.

The designer works with library of macro-cell which contain flip flop, a multiplexers etc., so need not to implement everything from simple logic gates.

QUESTIONS

1. Consider a logic gate representation of output Y_1, Y_2 for an inputs A&B is as below.



Gate Keyword → 3

IF A and B are in steady state, what's relationship between A, B, Y_1, Y_2 ?

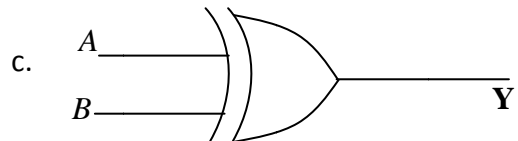
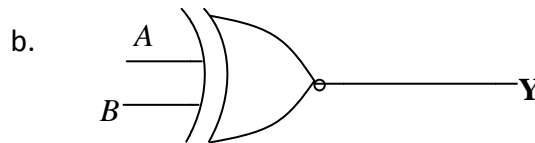
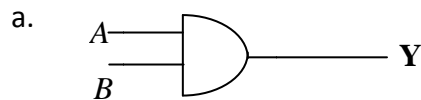
- a. $A = B = Y_1 = Y_2$ b. $A \neq B \neq Y_1 \neq Y_2$ c. $A = Y_2 = B = Y_1$ d. $A = Y_1 = \bar{B} = Y_2$

2. Consider a k-map shown below for two variable. Choose connect equivalent gate logic.

| | | |
|-----------|-----------|-----|
| | \bar{B} | B |
| \bar{A} | 1 | 0 |
| A | 0 | 1 |

Where, A=MSB, B=LSB

Gate Keyword → 2



3. Consider a logic where we have inputs A&B and output Y_1, Y_2, Y_3 ; It is expected that Y_1 should go high when $A > B$, Y_2 should go high when $A = B$, and Y_3 should go high $A < B$, what is expression for Y_1, Y_2, Y_3 ?

Gate Keyword → 5

a. $Y_1 = \bar{A}B$ $Y_2 = A \odot B$ $Y_3 = \bar{A}\bar{B}$

b. $Y_1 = \bar{A}\bar{B}$ $Y_2 = A \oplus B$ $Y_3 = \bar{A}B$

c. $Y_1 = \bar{A}\bar{B}$ $Y_2 = A \odot B$ $Y_3 = \bar{A}B$

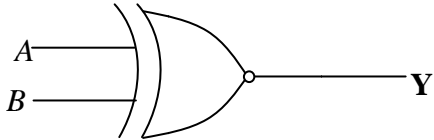
d. $Y_1 = \bar{A}B$ $Y_2 = A \odot B$ $Y_3 = \bar{A}\bar{B}$

SOLUTIONS

1. Answer: (c)

Solution: from figure shown above A and Y_1 tied together thus $A=Y_2$ similarly B and Y_1 are tied together hence $B= Y_1$ also A and Y_1 are complement of each other same case hold for Band Y_2 .

2. Answer: (b)

Solution: o\p of k-map = $\overline{A}B + AB = Y \Rightarrow$ 

3. Answer: (c)

Solution:

| A | B | Y_1 | Y_2 | Y_3 |
|---|---|-------|-------|-------|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 |

| | \overline{B} | B |
|----------------|----------------|---|
| \overline{A} | 0 | 0 |
| A | 1 | 0 |

$\overline{A}B$

| | \overline{B} | B |
|----------------|----------------|---|
| \overline{A} | 1 | 0 |
| A | 1 | 1 |

$A \odot B$

| | \overline{B} | B |
|----------------|----------------|---|
| \overline{A} | 0 | 1 |
| A | 0 | 0 |

$\overline{A}B$